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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,354	12/12/2003	Jin-Hwa Heo	8836-140 DIV (IE 10178-US	3563
22150	7590	07/05/2006	EXAMINER	
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			ANGADI, MAKI A	
			ART UNIT	PAPER NUMBER
			1765	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/734,354	Applicant(s) HEO ET AL.	
	Examiner Maki A. Angadi	Art Unit 1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/12/2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

- ✓ 1. Claims 9, 10, 15 and 16 are rejected under 35 U.S.C. 102 (b) over Rha (US Patent No. 6,127,241) in view of Yu (US Patent No. 5,801,083).

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reject

As to claim 9, Rha discloses a method of forming a trench isolation layer of a semiconductor device (col.1, lines 6-10) that includes the steps of:

Forming a trench-etching pattern for defining an active area on a substrate (20) (col.2, lines 59-61); Forming an isolation trench (33) on the substrate using the trench etching pattern as an etching mask (col.3, lines 48-51); Forming a silicon nitride liner (34) on a inner wall of the trench (col.3, lines 54-56)(Fig.3B); Forming a silicon oxide liner (35) on an inner side of the silicon nitride liner (col.4, lines 6-9)(Fig.3C); Partially filling the trench having the silicon oxide liner with a first buried layer (36) (col.4, lines 15-18) (Fig. 3D); Partially recessing an upper surface of the first buried layer by etching (col.4, lines 17-21); and Filling the trench by depositing the second buried layer on the first buried layer whose upper surface is partially recessed (col.4, lines 21-25).

Rha does not expressly disclose the heat treatment for hardening the silicon oxide liner. However, Yu discloses the heat treatment process for hardening silicon oxide layer (col.3, lines 56-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the heat treatment procedure in the trench isolation process used by Rha because Yu illustrates that heat treatment leads to the reduction of stress at the interface (col.3, lines 62-65).

As to claim 10, Rha discloses a step of forming a thermal oxide layer on the inner wall of the trench, between the step of forming the trench and the step of forming the silicon nitride layer (col.4, lines 6-11).

As to claim 15, Rha discloses the steps of exposing an upper part of the trench pattern, by removing the second buried layer with a planarization etching; and selectively removing the trench etching pattern (col.5, lines 23-34)).

As to claim 16, Rha discloses the step of etching the first buried layer, which is processed by wet etching (col.5, lines 27-30).

Claim Rejections - 35 USC § 103

2. Claim 11 is rejected under 35 U.S.C.102 (b) over Rha (US Patent No. 6,127,241) in view of Yu (US Patent No. 5,801,083) as applied to claim 9, in further view Oh (US Patent No. 6,187,651).

As to claim 11, Rha discloses the silicon oxide liner (34), which includes an HTO oxide layer (col.4, lines 6-9), and the heat treatment is performed at about 450°C. The annealing temperature disclosed by Rha is much lower than the value cited by the applicant. However, Oh discloses the heat treatment for shallow trench isolation structures in the temperature range of about 900°C (col.4, lines 24-27), which is within the range cited by the applicant. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the annealing temperature used by Rha because Oh illustrates that annealing at high temperatures leads to densification of undoped silicate

glass layer and prevent an over-recess condition from occurring due to the presence of trench (col.4, lines 22-24).

Claim Rejections - 35 USC § 103

3. Claims 12-14 are rejected under 35 U.S.C. 102 (b) over Rha (US Patent No. 6,127,241) in view of Yu (US Patent No. 5,801,083) as applied to claim 9, in further view of Zheng (US Patent No. 5,728,621) and Fukuyama (US Patent No. 5,770,260).

As to claim 12, Rha fails to disclose the step of filling the first buried layer with an SOG layer. However Zheng discloses the use of SOG layer (20) coated over the oxide layer (Fig.4) (col.2, lines 64-66). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select SOG layer in the STI process used by Rha because Zheng illustrates that the use SOG in the STI process allows for a thinner silicon nitride layer, thus resulting in a smaller height and less variation in the step height, leading to better planarization (col.2, lines 32-37).

Rha and Zheng fail to disclose the process of curing SOG layer into a silicon oxide layer. However, Fukuyama discloses a process of converting SOG layer into a silicon oxide layer by curing (col.3, lines 21-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to convert SOG layer into a silicon oxide layer for STI process used by Rha

because Fukuyama illustrates that the silicon oxide film obtained by curing SOG layer can be used at a greater thickness than an inorganic SOG material, and can make a base step sufficiently flat (col.1, lines 18-21).

As to claim 13, Rha fails to disclose the formation of the trench isolation layer wherein the SOG layer includes a polysilazane series material. However, Fukuyama discloses the SOG layer, which includes polysilazane material (col.3, lines 11-16), and curing step is performed at a temperature of about 300-450°C (Example 4, col.6) for about 3-30 minutes (Example 10, col.8). The temperature and time values are within the range cited by the applicant.

As to claim 14, Rha fails to disclose a method forming the trench isolation layer wherein the step of depositing the second buried layer includes HDP-CVD. However, Zheng discloses the step of depositing the second buried layer that included HDP-CVD (col.2, lines 42-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select HDP-CVD process because Zheng illustrates that HDP oxide is a more stable film and can fill a narrow trench without any weak spots (col.1, lines 32-36).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wood (US Patent No. 4,798,629) discloses spin-on glass for use in semiconductor processing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maki A. Angadi whose telephone number is 571-272-8213. The examiner can normally be reached on 8 AM to 4.30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Dr. Maki Angadi

Examiner

Art Unit 1765

NADINE WORTON
SUPERVISORY PATENT EXAMINER
ART UNIT 1765
